REMARKS

Initially, Applicants filed an Information Disclosure Statement (IDS) on January 19, 2005. The Examiner has not acknowledged receipt of this IDS. Applicants respectfully request that the Examiner consider the documents cited in connection with the IDS by initialing and returning a copy of the Form 1449 that accompanied the IDS.

In the non-final Office Action, the Examiner rejected claims 1, 4-7, 10-13, 16-19, and 22-24 under 35 U.S.C. § 102(e) as anticipated by Roy et al. (U.S. Patent No. 6,646,983); and rejected claims 2, 3, 8, 9, 14, 15, 20, 21, and 25-27 under 35 U.S.C. § 103(a) as unpatentable over Roy et al. in view of Ben-Zur et al. (U.S. Patent No. 6,754,174).

By this Amendment, Applicants amend claims 1, 10, 12, and 27 to improve form. Applicants respectfully traverse the Examiner's rejections under 35 U.S.C. §§ 102 and 103. Claims 1-27 remain pending.

In paragraph 2 of the Office Action, the Examiner rejected claims 1, 4-7, 10-13, 16-19, and 22-24 under 35 U.S.C. § 102(e) as allegedly anticipated by Roy et al. Applicants respectfully traverse the rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Roy et al. does not disclose or suggest the combination of features recited in claims 1, 4-7, 10-13, 16-19, and 22-24.

Independent claim 1, for example, is directed to an apparatus for interfacing a high-speed link to a network device. The apparatus comprises a receiver module, a framer module, and a

sprayer module. The receiver module operates at a first clock rate for receiving a stream of in-coming data from the high-speed link. The framer module operates at a second clock rate for deserializing the stream of in-coming data onto a multi-line bus and extracting data packets from the deserialized data on the multi-line bus, wherein the second clock rate is lower than the first clock rate. The sprayer module is configured to receive the extracted data packets from the framer module and, for each of the extracted data packets, select one of a plurality of processing paths in the network device and transmit the extracted data packet to the selected processing path.

Roy et al. does not disclose or suggest the combination of features recited in claim 1. For example, Roy et al. does not disclose or suggest a sprayer module that is configured to receive extracted data packets from a framer module and for each of the extracted data packets, select one of a plurality of processing paths in the network device and transmit the extracted data packet to the selected processing path.

The Examiner alleged that Roy et al. discloses a sprayer module and identified elements 16, 18, 20, and 22, and column 11, lines 2-8, of Roy et al. for support (Office Action, pages 2-3). Applicants respectfully disagree.

Roy et al. identifies element 16 as a pointer processor, element 18 as a path overhead (POH) processor, element 20 as an HDLC framer, and element 22 as a cell delineation block (col. 10, line 35, - col. 11, line 39). Roy et al. discloses that pointer processor 16 uses a SONET pointer to correctly locate the start of payload data being carried in a SONET envelope (col. 10, lines 35-37). Nowhere does Roy et al. disclose or suggest that pointer processor 16 receives extracted data packets from a framer module and, for each of the extracted data packets, selects

one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that POH processor 18 processes nine bytes of path overhead in each of forty-eight SONET SPEs (col. 10, lines 54-55). Nowhere does Roy et al. disclose or suggest that POH processor 18 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that HDLC framer 20 performs HDLC framing and forwards a PPP packet to a FIFO buffer, where it awaits assembly into PDUs (col. 11, lines 18-20). Nowhere does Roy et al. disclose or suggest that HDLC framer 20 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that cell delineation block 22 performs cell mapping as described in an ITU-T G.804 publication (col. 11, lines 29-31). Nowhere does Roy et al. disclose or suggest that cell delineation block 22 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Accordingly, Roy et al. does not disclose that any of pointer processor 16, POH processor 18, HDLC framer 20, and/or cell delineation block 22 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing

path, as required by claim 1. Therefore, even assuming, for the sake of argument, that it is reasonable to identify all of these elements as corresponding to the sprayer module recited in claim 1 (a point that Applicants do not concede), the sprayer module recited in claim 1 would not result.

The Examiner also identified column 11, lines 2-8, of Roy et al. as allegedly disclosing the sprayer module of claim 1 (Office Action, pages 2-3). Applicants respectfully disagree.

At column 10, line 66, through column 11, line 8, Roy et al. discloses:

> Once the frame boundaries of the incoming SONET/SDH signals are found and the location of the SPEs has been identified either through pointer processing or through Telecom bus I/F control signals, and the Path Overhead is processed, the payload is extracted from the SPE. The SPEs may be carrying TDM traffic, ATM cells or IP packets. The type of traffic for each SPE is configured through the microprocessor interface 78. Each SPE can carry only one type of traffic. The data from each SPE is routed directly to the correct payload extractor.

Contrary to the Examiner's allegation, nowhere in this section, or elsewhere, does Roy et al. disclose or suggest a sprayer module that is configured to receive extracted data packets from a framer module and for each of the extracted data packets, select one of a plurality of processing paths in the network device and transmit the extracted data packet to the selected processing path, as required by claim 1.

For at least the foregoing reasons, Applicants submit that claim 1 is not anticipated by Roy et al. Claims 4-7, 10, and 11 depend from claim 1 and are, therefore not anticipated by Roy et al. for at least the reasons given with regard to claim 1. Claims 4-7, 10, and 11 are also not anticipated by Roy et al. for reasons of their own.

For example, claim 4 recites that the plurality of processing paths includes a plurality of preprocessing modules for processing the extracted data packets. Roy et al. does not disclose or suggest the combination of features recited in claim 4.

The Examiner did not address the features of claim 4. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 4.

For at least these additional reasons, Applicants submit that claim 4 is not anticipated by Roy et al.

Claim 5 recites that the plurality of processing paths includes a plurality of switching/forwarding modules for switching or forwarding the extracted data packets. Roy et al. does not disclose or suggest the combination of features recited in claim 5.

The Examiner alleged that Roy et al. discloses a plurality of switching/forwarding modules and identified elements 16, 18, 20, and 22, and column 11, lines 2-8, of Roy et al. for support (Office Action, page 3). Applicants respectfully disagree.

The Examiner identified elements 16, 18, 20, and 22 as allegedly corresponding to the sprayer module recited in claim 1 and then alleged that these exact same elements correspond to a plurality of switching/forwarding modules recited in claim 5. Applicants submit that such an allegation lacks merit.

Under the Examiner's reasoning, Roy et al. allegedly discloses that elements 16, 18, 20, and 22 receive extracted data packets from a framer module and, for each of the extracted data packets, select one of a plurality of elements 16, 18, 20, and 22, which switches or forwards the extracted data packets, in the network device and transmit the extracted data packet to the selected element 16, 18, 20, and 22. Nothing in Roy et al. supports the Examiner's allegation.

For at least these additional reasons, Applicants submit that claim 5 is not anticipated by Roy et al.

Claim 6 recites that the sprayer module is configured to transmit each extracted data packet to one of the plurality of preprocessing modules based on a load balancing technique. Roy et al. does not disclose or suggest the combination of features recited in claim 6.

The Examiner alleged that Roy et al. discloses the features of claim 6 and cited column 12, lines 7-28, of Roy et al. for support (Office Action, page 3). Applicants respectfully disagree.

At column 12, lines 7-28, Roy et al. discloses:

> The descriptor constructor 64 determines whether the data is an ATM cell or an IP packet and generates a corresponding interrupt to trigger the IPF/ATM look-up processor 66 to perform either IP routing look-up or ATM look-up. IP routing look-up is performed by searching for the IP destination address for every packet and the IP source address for packets that need classification. ATM look-up is performed by searching the VPI/VCI fields of the cells. Outputs of the IPF/ATM look-up processor 66 for both IP packets and ATM cells include a seventeen-bit flow index, a five-bit QOS index, and an indicator showing whether the IP packet needs classification. If the IP packet needs classification, the packet is passed to the IP classification processor 68 for classification; otherwise it is passed to the next stage of packet processing, the RED/policing processor 70. IP classification is described in detail in section 6.4 of Appendix A. The RED/Policing processor 70 performs random early detection and weighted random early detection for IP congestion control, performs leaky bucket policing for ATM traffic control, and performs early packet and partial packet discard for controlling ATM traffic which contains packets.

This section of Roy et al. describes descriptor constructor 64, IPF/ATM look-up processor 66, IP classification processor 68, and RED/policing processor 70. Nowhere in this section does Roy et al. disclose or suggest any of the elements that the Examiner alleged were the equivalent of the sprayer module. The Examiner alleged that elements 16, 18, 20, and 22 correspond to the sprayer, and nowhere in this section does Roy et al. disclose anything relating to elements 16, 18, 20, and 22.

Nevertheless, nowhere in the section identified by the Examiner, or any other section, does Roy et al. disclose or suggest a sprayer module that transmits each extracted data packet to

one of a plurality of preprocessing modules based on a load balancing technique. In fact, Roy et al. does not even mention load balancing.

For at least these additional reasons, Applicants submit that claim 6 is not anticipated by Roy et al.

Claim 11 recites a desprayer module for receiving data packets from the plurality of processing paths and transmitting the received data packets to the deframer module. Roy et al. does not disclose or suggest the combination of features recited in claim 11.

The Examiner alleged that Roy et al. discloses a desprayer module and identified elements 136 and 138 and column 19, lines 4-13, of Roy et al. for support (Office Action, page 4). Applicants respectfully disagree.

Roy et al. identifies element 136 as a link data stream mapper and element 138 as a link data stream serializer (col. 18, line 49, - col. 19, line 29). Roy et al. discloses that link data stream mapper 136 inserts data and request elements into outgoing serial data links (col. 18, lines 49-50). Nowhere does Roy et al. disclose or suggest that link data stream mapper 136 receives data packets from a plurality of processing paths and transmits the received data packets to a deframer module (which the Examiner alleged corresponds to element 40 in Fig. 1A of Roy et al.), as required by claim 11.

Roy et al. discloses that link data stream serializer 138 creates an output link serial stream by splitting a row data stream into two streams for transmission on two paths (col. 19, lines 12-17). Nowhere does Roy et al. disclose or suggest that link data stream serializer 138 receives data packets from a plurality of processing paths and transmits the received data packets to a

deframer module (which the Examiner alleged corresponds to element 40 in Fig. 1A of Roy et al.), as required by claim 11.

For at least these additional reasons, Applicants submit that claim 11 is not anticipated by Roy et al.

Independent claim 12 is directed to an apparatus for interfacing at least one line interface card to a plurality of switching/forwarding modules of a network device. The apparatus comprises a plurality of preprocessing modules for processing data packets and transmitting the processed data packets to respective switching/forwarding modules, and a sprayer module for receiving data packets from at least one line interface card and, for each received data packet, selecting one of the plurality of preprocessing modules and transmitting the received data packet to the selected preprocessing module.

Roy et al. does not disclose or suggest the combination of features recited in claim 12. For example, Roy et al. does not disclose or suggest a sprayer module for receiving data packets from at least one line interface card and, for each received data packet, selecting one of the plurality of preprocessing modules and transmitting the received data packet to the selected preprocessing module.

The Examiner alleged that Roy et al. discloses a sprayer module and identified elements 16, 18, 20, and 22, and column 11, lines 2-8, of Roy et al. for support (Office Action, page 4). Applicants respectfully disagree.

Roy et al. identifies element 16 as a pointer processor, element 18 as a path overhead (POH) processor, element 20 as an HDLC framer, and element 22 as a cell delineation block (col. 10, line 35, - col. 11, line 39). Roy et al. discloses that pointer processor 16 uses a SONET

pointer to correctly locate the start of payload data being carried in a SONET envelope (col. 10, lines 35-37). Nowhere does Roy et al. disclose or suggest that pointer processor 16 receives data packets from at least one line interface card and, for each received data packet, selects one of the plurality of preprocessing modules and transmits the received data packet to the selected preprocessing module, as required by claim 12.

Roy et al. discloses that POH processor 18 processes nine bytes of path overhead in each of forty-eight SONET SPEs (col. 10, lines 54-55). Nowhere does Roy et al. disclose or suggest that POH processor 18 receives data packets from at least one line interface card and, for each received data packet, selects one of the plurality of preprocessing modules and transmits the received data packet to the selected preprocessing module, as required by claim 12.

Roy et al. discloses that HDLC framer 20 performs HDLC framing and forwards a PPP packet to a FIFO buffer, where it awaits assembly into PDUs (col. 11, lines 18-20). Nowhere does Roy et al. disclose or suggest that HDLC framer 20 receives data packets from at least one line interface card and, for each received data packet, selects one of the plurality of preprocessing modules and transmits the received data packet to the selected preprocessing module, as required by claim 12.

Roy et al. discloses that cell delineation block 22 performs cell mapping as described in an ITU-T G.804 publication (col. 11, lines 29-31). Nowhere does Roy et al. disclose or suggest that cell delineation block 22 receives data packets from at least one line interface card and, for each received data packet, selects one of the plurality of preprocessing modules and transmits the received data packet to the selected preprocessing module, as required by claim 12.

Accordingly, Roy et al. does not disclose that any of pointer processor 16, POH processor 18, HDLC framer 20, and/or cell delineation block 22 receives data packets from at least one line interface card and, for each received data packet, selects one of the plurality of preprocessing modules and transmits the received data packet to the selected preprocessing module, as required by claim 12. Therefore, even assuming, for the sake of argument, that it is reasonable to identify all of these elements as corresponding to a sprayer module (a point that Applicants do not concede), the sprayer module recited in claim 12 would not result.

The Examiner also identified column 11, lines 2-8, of Roy et al. as allegedly disclosing the sprayer module of claim 12 (Office Action, page 4). Applicants respectfully disagree.

Column 10, line 66, through column 11, line 8, of Roy et al. has been reproduced above. Contrary to the Examiner's allegation, nowhere in this section, or elsewhere, does Roy et al. disclose or suggest a sprayer module that is configured to receive data packets from at least one line interface card and, for each received data packet, select one of the plurality of preprocessing modules and transmit the received data packet to the selected preprocessing module, as required by claim 12.

For at least the foregoing reasons, Applicants submit that claim 12 is not anticipated by Roy et al. Claims 13 and 16 depend from claim 12 and are, therefore, not anticipated by Roy et al. for at least the reasons given with regard to claim 12. Claims 13 and 16 also recite features similar to features recited in claims 4-7, 10, and 11. Claims 13 and 16 are, therefore, also not anticipated by Roy et al. for at least reasons similar to reasons given with regard to claims 4-7, 10, and 11.

Independent claim 17 is directed to a networking device. The networking device comprises a sprayer module, a plurality of preprocessing modules, and a plurality of switching/forwarding modules. The sprayer module is for receiving data packets and, for each of the data packets, selecting one of a plurality of channels and outputting the data packet on the selected channel. The plurality of preprocessing modules are for processing data packets. Each preprocessing module receives data packets from one of the channels of the sprayer module. Each switching/forwarding module receives data packets from a corresponding one of the plurality of preprocessing modules.

Roy et al. does not disclose or suggest the combination of features recited in claim 17. For example, Roy et al. does not disclose or suggest a sprayer module for receiving data packets and, for each of the data packets, selecting one of a plurality of channels and outputting the data packet on the selected channel.

The Examiner alleged that Roy et al. discloses a sprayer module and identified elements 16, 18, 20, and 22, and column 11, lines 2-8, of Roy et al. for support (Office Action, page 5). Applicants respectfully disagree.

Roy et al. identifies element 16 as a pointer processor, element 18 as a path overhead (POH) processor, element 20 as an HDLC framer, and element 22 as a cell delineation block (col. 10, line 35, - col. 11, line 39). Roy et al. discloses that pointer processor 16 uses a SONET pointer to correctly locate the start of payload data being carried in a SONET envelope (col. 10, lines 35-37). Nowhere does Roy et al. disclose or suggest that pointer processor 16 receives data packets and, for each of the data packets, selects one of a plurality of channels and outputs the data packet on the selected channel, as required by claim 17.

Roy et al. discloses that POH processor 18 processes nine bytes of path overhead in each of forty-eight SONET SPEs (col. 10, lines 54-55). Nowhere does Roy et al. disclose or suggest that POH processor 18 receives data packets and, for each of the data packets, selects one of a plurality of channels and outputs the data packet on the selected channel, as required by claim 17.

Roy et al. discloses that HDLC framer 20 performs HDLC framing and forwards a PPP packet to a FIFO buffer, where it awaits assembly into PDUs (col. 11, lines 18-20). Nowhere does Roy et al. disclose or suggest that HDLC framer 20 receives data packets and, for each of the data packets, selects one of a plurality of channels and outputs the data packet on the selected channel, as required by claim 17.

Roy et al. discloses that cell delineation block 22 performs cell mapping as described in an ITU-T G.804 publication (col. 11, lines 29-31). Nowhere does Roy et al. disclose or suggest that cell delineation block 22 receives data packets and, for each of the data packets, selects one of a plurality of channels and outputs the data packet on the selected channel, as required by claim 17.

Accordingly, Roy et al. does not disclose that any of pointer processor 16, POH processor 18, HDLC framer 20, and/or cell delineation block 22 receives data packets and, for each of the data packets, selects one of a plurality of channels and outputs the data packet on the selected channel, as required by claim 17. Therefore, even assuming, for the sake of argument, that it is reasonable to identify all of these elements as corresponding to a sprayer module (a point that Applicants do not concede), the sprayer module recited in claim 17 would not result.

The Examiner also identified column 11, lines 2-8, of Roy et al. as allegedly disclosing the sprayer module of claim 17 (Office Action, page 5). Applicants respectfully disagree.

Column 10, line 66, through column 11, line 8, of Roy et al. has been reproduced above. Contrary to the Examiner's allegation, nowhere in this section, or elsewhere, does Roy et al. disclose or suggest a sprayer module that is configured to receive data packets and, for each of the data packets, select one of a plurality of channels and output the data packet on the selected channel, as required by claim 17.

Furthermore, the Examiner's rejection with regard to claim 17 is faulty. For example, the Examiner identified the same elements (16, 18, 20, and 22) of Roy et al. as allegedly corresponding to the sprayer module, the plurality of preprocessing modules, and the plurality of switching/forwarding modules recited in claim 17 (Office Action, page 5). Such an allegation is unreasonable. If the Examiner maintains this allegation, Applicants respectfully request that the Examiner explain, in detail, how elements 16, 18, 20, and 22 can be equated to each of the sprayer module, a plurality of preprocessing modules, and the plurality of switching/forwarding modules and how these same elements 16, 18, 20, and 22 can be equated to all of the sprayer module, a plurality of preprocessing modules, and the plurality of switching/forwarding modules.

For at least the foregoing reasons, Applicants submit that claim 17 is not anticipated by Roy et al. Claims 18, 19, and 22-24 depend from claim 17 and are, therefore, not anticipated by Roy et al. for at least the reasons given with regard to claim 17. Claims 18, 19, and 22-24 also recite features similar to features recited in claims 4-7, 10, and 11. Claims 18, 19, and 22-24 are, therefore, also not anticipated by Roy et al. for at least reasons similar to reasons given with regard to claims 4-7, 10, and 11.

In view of the foregoing, Applicants respectfully submit that claims 1, 4-7, 10-13, 16-19, and 22-24 are not anticipated by Roy et al.

In paragraph 4 of the Office Action, the Examiner rejected claims 2, 3, 8, 9, 14, 15, 20, 21, and 25-27 under 35 U.S.C. § 103(a) as allegedly unpatentable over Roy et al. in view of Ben-Zur et al. Applicants respectfully traverse the Examiner's rejection.

Claims 2, 3, 8, 9, 14, 15, 20, 21, 25, and 26 variously depend from claims 1, 12, and 17. The disclosure of Ben-Zur et al. does not cure the deficiencies in the disclosure of Roy et al. identified above with regard to claims 1, 12, and 17. Therefore, claims 2, 3, 8, 9, 14, 15, 20, 21, 25, and 26 are patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 1, 12, and 17. Claims 2, 3, 8, 9, 14, 15, 20, 21, 25, and 26 are further patentable over Roy et al. and Ben-Zur et al. for reasons of their own.

For example, claim 8 recites that the receiver module, the framer module, the sprayer module, the plurality of preprocessing modules, and the plurality of memories are mounted onto a single board. Neither Roy et al. nor Ben-Zur et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 8.

The Examiner admitted that Roy et al. does not disclose the features of claim 8, but alleged that Ben-Zur et al. discloses these features and cited column 5, lines 18-21, of Ben-Zur et al. for support (Office Action, pages 7-8). Applicants respectfully disagree.

Ben-Zur et al. does not disclose or suggest anything similar to the receiver module, framer module, sprayer module, plurality of preprocessing modules, and/or plurality of memories recited in claim 8. Therefore, Ben-Zur et al. cannot disclose a receiver module, framer module, sprayer module, plurality of preprocessing modules, and plurality of memories mounted onto a single board, as required by claim 8.

In addition, at column 5, lines 18-21, Ben-Zur et al. discloses:

> The TMO switch of an embodiment is a data optimized SONET platform that integrates SONET ADMs, DCSs and ATM/FR switch functionality into a single platform using common card architecture.

Nowhere in this section does Ben-Zur et al. disclose a set of elements mounted onto a single board, let alone a receiver module, framer module, sprayer module, plurality of preprocessing modules, and plurality of memories mounted onto a single board, as required by claim 8.

For at least these additional reasons, Applicants submit that claim 8 is patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination.

Claim 9 recites that the receiver module, the framer module, the sprayer module, the plurality of preprocessing modules, and the plurality of memories are integrated onto a single chip. Neither Roy et al. nor Ben-Zur et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 9.

The Examiner admitted that Roy et al. does not disclose the features of claim 9, but alleged that Ben-Zur et al. discloses these features and cited column 15, lines 39-44, of Ben-Zur et al. for support (Office Action, page 8). Applicants respectfully disagree.

Ben-Zur et al. does not disclose or suggest anything similar to the receiver module, framer module, sprayer module, plurality of preprocessing modules, and/or plurality of memories recited in claim 8. Therefore, Ben-Zur et al. cannot disclose a receiver module, framer module, sprayer module, plurality of preprocessing modules, and plurality of memories integrated onto a single chip, as required by claim 9.

In addition, at column 15, lines 39-44, Ben-Zur et al. discloses:

> The CPU proceeds to the area of the associated FPGA containing the unit registers 1702. The FPGA can be located on a particular card of the TMO switch or can be distributed

> among a number of cards of the TMO switch. In an embodiment, the FPGA is located on a cross-connect card coupled to the CCC hosting the CPU, but is not so limited.

Nowhere in this section does Ben-Zur et al. disclose a set of elements integrated onto a single chip, let alone a receiver module, framer module, sprayer module, plurality of preprocessing modules, and plurality of memories integrated onto a single chip, as required by claim 9.

For at least these additional reasons, Applicants submit that claim 9 is patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination.

Claims 14 and 15 recite features similar to features recited in claims 8 and 9, respectively. Claims 14 and 15 are, therefore, also patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination, for at least reasons similar to reasons given with regard to claims 8 and 9.

Independent claim 27 is directed to a method of receiving data from a high-speed link. The method comprises receiving a stream of data signals at a data rate of at least approximately 10 Gigabits per second; deserializing the stream of data signals onto a multi-line bus; extracting data packets from the deserialized data; and spraying the data packets across a plurality of processing paths according to a load balancing or hashing technique.

Neither Roy et al. nor Ben-Zur et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 27. For example, neither Roy et al. nor Ben-Zur et al. discloses or suggests spraying data packets across a plurality of processing paths according to a load balancing or hashing technique.

The Examiner alleged that Roy et al. discloses this feature and cited column 12, lines 7-28, of Roy et al. for support (Office Action, page 9). Applicants respectfully disagree.

Column 12, lines 7-28, of Roy et al. has been reproduced above. Nowhere in this section, or elsewhere, does Roy et al. disclose or suggest spraying data packets across a plurality of processing paths according to a load balancing or hashing technique. In fact, Roy et al. does not even mention load balancing or hashing. The disclosure of Ben-Zur et al. provides nothing to cure these deficiencies in the disclosure of Roy et al.

For at least these reasons, Applicants submit that claim 27 is patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination.

In view of the foregoing, Applicants respectfully submit that claims 2, 3, 8, 9, 14, 15, 20, 21, and 25-27 are patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination.

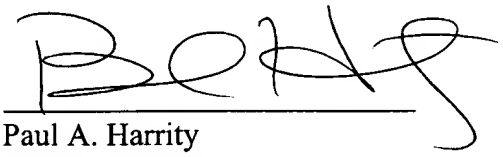
In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of the application and the timely allowance of pending claims 1-27.

To the extent necessary, a petition for an extension of time under 35 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: 

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